REMARKS/ARGUMENTS

Applicant has received the Office Action dated October 3, 2005, (hereinafter the "*Office Action*") which: 1) rejects claims 1, 5, and 12 under 35 U.S.C. § 112, 2nd paragraph, as allegedly indefinite; and 2) rejects claims 1-19 under 35 U.S.C. § 102 (e) as allegedly anticipated by *Tsunoda et al.* (U.S. Pub. No. 2003/0028733, hereinafter "*Tsunoda*").

With this Response, Applicant amends claims 1, 5, 7, 10, 12, 14, 15, and 18 and cancels claim 9 and 13.[1] Therefore, claims 1-8, 10-12, and 14-19 remain pending.

I. § 112 REJECTIONS

Claims 1, 5, and 12 stand rejected as allegedly indefinite for failing to point out and distinctly claim the invention. With this Response, Applicant amends claims 1, 5, and 12 in an effort to rectify any alleged indefiniteness issues cited in the *Office Action*. Specifically, Applicant amends claims 1 and 5 so that references to the "memory array" refer to the nonvolatile memory array at line 2 of claim 1. Further, Applicant amends claim 5 to indicate that "the associated region" recited in the last line of claim 5 has antecedent basis in the different associated regions from line 3 of claim 5.[2] Lastly, Applicant amends claim 12 to indicate that the acts recited in claim 12 occur prior to the act of "detecting a pending power-down" recited in line 2 of claim 10. Accordingly, Applicant respectfully requests withdrawal of the § 112 rejections.

II. § 102 REJECTIONS

The pending claims stand rejected under § 102 as allegedly anticipated by *Tsunoda*. Applicant respectfully traverses because *Tsunoda* fails to teach or suggest all of the claim elements.

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[1] This cancellation of claims should not be construed as a concession by Applicant as to the correctness of the assertions in the *Office Action*. Further, Applicant reserves the right to reassert these canceled claims later in prosecution.

[2] Although not cited in the *Office Action*, claim 18 contained language similar to claim 5 with regard to "the associated region," and therefore Applicant similarly amends claim 18.

A. Claim 1

Applicant respectfully submits that *Tsunoda* fails to teach or suggest all of the elements of claim 1. For example, independent claim 1, as amended, recites "a table memory configured to indicate one or more addresses within the nonvolatile memory array that have been recently accessed." *Tsunoda* fails to teach or suggest indicating one or more addresses within the nonvolatile memory that have been recently accessed. Thus, independent claim 1, and its dependent claims, are patentable over *Tsunoda* for at least this reason. Independent claims 1, 10, 14, and 15 contain similar claim elements and therefore, independent claims 1, 10, 14, and 15, as well as their dependent claims, are patentable over *Tsunoda* for at least the same reason as claim 1.

Tsunoda is deficient in other regards as well. For example, claim 1 requires that the nonvolatile buffered memory interface be integrated on a substrate with the nonvolatile memory array. The *Office Action* recognizes this requirement of claim 1, and contends that *Tsunoda* at ¶¶[0056] and [0124] teach this recited claim element. *Office Action* at 4-5. Unfortunately, a more detailed study of *Tsunoda* suggests otherwise or suggests at the very least that portions of *Tsunoda* are directly contradictory to this requirement. Paragraph [0056] (which is cited in the *Office Action*) specifically notes that memory 4000 includes the SDRAM 4010 (the volatile memory) and the flash memory 4020 (the nonvolatile memory), which are "**on different silicon chips.**" That is, instead of the volatile memory being integrated on substrate with the nonvolatile memory (as required by claim 1) the volatile and nonvolatile memories of memory 4000 are on separate substrates. Paragraph [0124] of Tsunoda (which is also cited in the *Office Action*) notes that "memory apparatus 101, 901, 1301, and 1401 ... may be housed on one semiconductor chip," however, this teaching certainly does not apply to memory 4000, which is discussed at length in ¶¶[0038]-[0095] of *Tsunoda*. Ultimately, over half of the teachings of *Tsunoda* are directly contrary to the language of claim 1, and therefore, Applicant respectfully submits that reliance on these portions in rejecting the claims is improper.

B. Claim 7

In addition to being patentable over *Tsunoda* for at least some of the reasons stated above with regard to claim 1, *Tsunoda* similarly fails to teach or suggest all of the claim elements of claim 7. For example, claim 7 requires that "wherein the interface control module is coupled to the memory array ... to prepare read buffers to satisfy anticipated read commands." Although the *Office Action* cites ¶[0107] as allegedly teaching this claim element, there simply is no teaching or suggestion of anticipated read commands. Thus, *Tsunoda* does not teach or suggest that the interface control module prepares read buffers to satisfy anticipated read commands, and Applicant respectfully submits that claim 7 is patentable over *Tsunoda* for at least this additional reason.

Furthermore, page 11 of the *Office Action* specifies that claim 7 is interpreted to mean that "the memory array comprises magnetic random access memory (MRAM)." Applicant respectfully notes that such a position is in error and effectively amounts to the prohibited practice of reading non-recited claim elements into the claims. *See MPEP* § 2111. Indeed, if Applicant had intended claim 7 to include MRAM, such an element would have been originally included in the claim. Accordingly, Applicant respectfully requests reconsideration of any such "interpretation" of claim 7 that requires the memory array to include MRAM.

III. CONCLUSION

In the course of the foregoing discussions, Applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents

accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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